REMARKS

Applicant acknowledges the withdrawal of claims 3-5 and 8-10 as being drawing to a non-elected species pursuant to the restriction requirement dated March 2, 2004.

The rejection of claims 1, 2, 6 and 7 under 35 USC 103(a) as being upatentable over Horino et al, taken alone or in combination with either Ando et al or JP 9-270137 is respectfully traversed.

The Horino et al reference is cited as the primary reference in the rejection of claims 1, 2, 6 and 7. This reference has an effective filing date of December 27, 1999, which is subsequent to the filing date of the parent application JP11-266090, to which applicant has claimed priority. Applicant has attached hereto a certified English translation of the priority document to perfect applicants claim to priority. Accordingly, the rejection of claims 1, 2 and 6 and 7 should now be withdrawn.

If for any reason the Examiner disagrees with applicant regarding applicants claim to priority, it is requested that the Examiner call applicants attorney at 212-278-1307 to discuss what the Examiner deems to be missing from applicants perfection of the priority claim.

Assuming the attached certified translation of the priority document satisfies the requirements of 37 CFR 1.55, the reference to Horino et al is no longer prior art defeating the rejection of the claims under 35 USC 103(a) based upon Horino et al. Accordingly, the application should now be in condition for allowance.

Reconsideration and allowance of claims 1, 2 and 6 and 7 is respectfully solicited.

Respectfully submitted,

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MAILING CERTIFICATE

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as first class mail in an envelope addressed to Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450: on August 2, 2005.

I, Tadahiko Itoh, a Patent Attorney of Tokyo, Japan having my office at 32nd Floor, Yebisu Garden Place Tower, 20-3 Ebisu 4-Chome, Shibuya-Ku, Tokyo 150-6032, Japan do solemnly and sincerely declare that I am the translator of the attached English language translation and certify that the attached English language translation is a correct, true and faithful translation of Japanese Patent Application No. 11-266090 to the best of my knowledge and belief.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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JUN. 23. 2005

PATENT OFFICE
JAPANESE GOVERNMENT

This is to certify that the annexed is a true copy of the following application as filed with this office.

Date of Application: September 20, 1999

Application Number: Japanese Patent Application No. 11-266090

Applicant(s): TEAC CORPORATION

September 8, 2000

Commissioner,
Patent Office Kouzo Oikawa (Seal)

Certificate No.2000-3071369

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(Document Name)	Specification 1
(Document Name)	Drawing 1
(Document Name)	Abstract 1

[DOCUMENT NAME] SPECIFICATION

[TITLE OF THE INVENTION] WOBBLE SIGNAL DETECTION CIRCUIT OF AN OPTICAL DISK APPARATUS

[PATENT CLAIMS]

1. A wobble signal detection circuit of an optical disk apparatus which detects a wobble signal by emitting a light beam spot onto a pregroove on an optical disk during recording and reproduction, characterized by comprising:

photodetection means for performing photodetection of each of right and left parts of the light beam spot divided in a longitudinal direction of a track, the light beam spot being emitted onto the optical disk;

sample-and-hold means for sampling and holding right and left detection signals detected by said photodetection means at a time of recording;

lowpass filter means for removing a noise component generated by the sampling from each of right and left signals output by said sample-and-hold means; and

subtraction means for obtaining the wobble signal by calculating a difference between right and left signals output by said lowpass filter means.

2. The wobble signal detection circuit of the optical disk apparatus as claimed in claim 1, characterized by comprising:

gain adjustment means in place of said lowpass filter means,

said gain adjustment means adjusting the noise components generated by sampling the right and left signals output by said sample-and-hold means so that the noise components are substantially equal in level, and supplying the right and left signals to said subtraction means.

[DETAILED DESCRIPTION OF THE INVENTION]

[0001]

[TECHNICAL FIELD OF THE INVENTION]

The present invention relates generally to a wobble signal detection circuit of an optical disk apparatus, and more particularly to a wobble signal detection circuit of an optical disk apparatus detecting an ATIP signal from an optical disk such as a CD-R disk.

[0002]

[PRIOR ART]

Optical disks of a direct-read-after-write type include two types: write-once and erasable. Of these, with respect to a write-once optical disk, there are methods such as forming a pit by using tellurium (Te) or bismuth (Bi) as the material of a signal recording surface and melting it by emitting a light beam, and using Sb_2Se_3, TeO_x or a thin film of organic dye as the material of a recording surface and altering light reflectivity by emitting a light beam.

[0003]

A CD-R disk, which is a write-once optical disk, includes a pregroove for guiding. The pregroove wobbles slightly radially at a center frequency of 22.05 kHz. Address information during recording called ATIP (Absolute Time In Pregroove) is multiplexed and recorded in the pregroove by frequency shift keying (FSK) with a maximum deviation of ±1 kHz.

[0004]

In the CD-R disk, the ATIP information is detected by reproducing a wobble signal of the above-mentioned center frequency of 22.05 kHz at the time of both recording and reproduction. At the time of recording, the ATIP information is employed to confirm a recording position.

Here, the ATIP information is detected in the following three modes. The first one is an unrecorded disk reproduction mode, the second one is a reproduction-during-recording mode, and the third one is a recorded disk reproduction mode.

[0005]

FIG. 5 shows a block diagram of a conventional wobble signal detection circuit. Here, a light beam spot 11 is emitted onto a pregroove 10 shown in FIG. 2, and its reflected beam is detected by four divided detectors 12A, 12B, 12C, and 12D. The detection signals A, B, C, and D of these detectors 12A, 12B, 12C, and 12D, respectively, are supplied to a sample-and-hold circuit 14 of FIG. 5.

[0006]

The sample-and-hold circuit 14 is turned off in the first unrecorded disk reproduction mode and the third recorded disk reproduction mode so as to let the supplied signals pass and to output them, and is turned on in the second reproduction-during-recording mode so as to output sampled and held signals. The signals A and B from the detectors 12A and 12B on the left side in the longitudinal direction of a track (that is, the pregroove 10), output by the sample-and-hold circuit 14, are added in an adder 16, and the signals C and D from the detectors 12C and 12D on the right side in the longitudinal direction of the track, output by the sample-and-hold circuit 14, are added in an adder 18.

[0007]

The output signals (A+B) and (C+D) of the adders 16 and 18, respectively, are supplied via capacitors C1 and C2 to a subtracter 20, where the output signal of the adder 18 is subtracted from the output signal (A+B) of the adder 16, so that a signal (A+B) - (C+D) is supplied to a

terminal a of a switch 22. In the first unrecorded disk reproduction mode, the terminal a of the switch 22 is selected. The output of the subtracter 20 is supplied to a bandpass filter (BPF) 24, where unnecessary frequency components are removed, and is further supplied via a coupling capacitor C3 to a highpass filter (HPF) 26, where unnecessary frequency components are removed. Thereafter, it is compared with a reference voltage Vref in a comparator 28, so that a binary wobble signal (A+B) - (C+D) is obtained and output from a terminal 32.

[0008]

On the other hand, in the third recorded disk reproduction mode, a terminal b of the switch 22 is selected. Here, the output signal of the adder 16 including an reproduced RF signal is supplied to a VCA (voltage-controlled amplifier) 34, while the output signal of the adder 18 including the reproduced RF signal is supplied to a VCA (voltage-controlled amplifier) 36. An AGC (automatic gain control circuit) 35 performs feedback control so that the amplitude of the output signal of the VCA 34 is at a predetermined level. Similarly, an AGC (automatic gain control circuit) 37 performs feedback control so that the amplitude of the output signal of the VCA 36 is at a predetermined level.

[0009]

A subtracter 38 subtracts the output signal (C+D+RF) of the VCA 36 from the output signal (A+B+RF) of the VCA 34. At this point, the reproduced RF signals equally included in the respective signals A, B, C, and D offset each other, and a signal (A+B) - (C+D) is supplied to the terminal b of the switch 22. In the third recorded disk reproduction mode, the terminal b of the switch 22 is selected, so that it is supplied to the bandpass filter 24,

where unnecessary frequency components are removed, and is further supplied via the coupling capacitor C3 to the highpass filter 26, where unnecessary frequency components are removed. Thereafter, it is compared with the reference voltage Vref in the comparator 28, so that a binary wobble signal (A+B) - (C+D) is obtained and output from the terminal 32.

[0010]

Further, in the second reproduction-during-recording mode, the sample-and-hold circuit 14 is turned on and the terminal a of the switch 22 is selected. During recording, light beam power alternately repeats write power (a maximum value) and read power (a minimum value) as shown in FIG. 3(A), and the sample-and-hold circuit 14 samples and holds a signal of a reproduction level at the time of read power shown in FIG. 3(B) with an enlarged time axis at the rising of sampling pulses shown in FIG. 3(C). Here, the output signals of the sample-and-hold circuit 14 include noise generated by the sampling, so that the output signals of the adders 16 and 18 are as shown in FIGS. 3(D) and (E). Here, the noise generated by the sampling includes noise generated by read light fluctuation that is caused when the light beam power changes from write power to read power. Further, in rewritable disks such as CD-RW disks, at the time of overwriting, a signal component previously recorded on the disk may appear as noise at the time of sampling, and this noise component is also included. However, by subtraction of both signals in the subtracter 20, the noises generated by the sampling offset each other, so that a signal (A+B) - (C+D) as shown in FIG. 3(F) is obtained. This signal is selected by the switch 22 so as to be supplied to the bandpass filter 24, where unnecessary frequency components

are removed. This signal is further supplied via the coupling capacitor C3 to the highpass filter 26, where unnecessary frequency components are removed. Thereafter, it is compared with the reference voltage Vref in the comparator 28, so that a binary wobble signal (A+B) - (C+D) is obtained and output from the terminal 32.

[0011]

[PROBLEMS TO BE SOLVED BY THE INVENTION]

However, the sample-and-hold circuit 14 includes variations in the gain and offset, so that respective errors are caused. Therefore, the magnitudes of the sampling noises generated in the sample-and-hold waveforms of the detectors 12A, 12B, 12C and 12D are not uniform. For example, when the sampling noise included in the output signal of the adder 16 shown in FIG. 6(A) is greater than the sampling noise included in the output signal of the adder 18 shown in FIG. 6(B), the sampling noise components do not offset each other completely even if subtraction is performed in the subtracter 20, so that the output signal of the subtracter 20 includes sampling noise as shown in FIG. 6(C). This sampling noise increases as sampling and holding is performed at higher speed. Therefore, when recording speed becomes high, this sampling noise cannot be ignored, so that there arises the problem of a decrease in the performance of reproduction of ATIP information from a wobble signal.

[0012]

The present invention is made in view of the above-described point, and has an object of providing a wobble signal detection circuit of an optical disk unit which can effectively remove sampling noise from a wobble signal in the reproduction-during-recording mode and improve the performance of reproduction of ATIP information.

[0013]

[MEANS FOR SOLVING THE PROBLEMS]

The invention recited in claim 1 has, in a wobble signal detection circuit of an optical disk apparatus which detects a wobble signal by emitting a light beam spot onto a pregroove on an optical disk during recording and reproduction,

photodetection means for performing photodetection of each of right and left parts of the light beam spot divided in a longitudinal direction of a track, the light beam spot being emitted onto the optical disk;

sample-and-hold means for sampling and holding right and left detection signals detected by the photodetection means at a time of recording;

lowpass filter means for removing a noise component generated by the sampling from each of right and left signals output by the sample-and-hold means; and

subtraction means for obtaining the wobble signal by calculating a difference between right and left signals output by the lowpass filter means.

[0014]

Thus, at the time of recording, a sampling noise component is removed from each of right and left signals output by sample-and-hold means, and a wobble signal is calculated from the right and left signals. Accordingly, it is possible to remove the sampling noise of a wobble signal effectively, and to improve the performance of reproduction of ATIP information.

The invention recited in claim 2 has, in the wobble signal detection circuit of the optical disk apparatus as recited in claim 1,

gain adjustment means in place of said lowpass filter means, the gain adjustment means adjusting the

noise components generated by sampling the right and left signals output by the sample-and-hold means so that the noise components are substantially equal in level, and supplying the right and left signals to the subtraction means.

[0015]

Thus, the noise components generated by sampling the right and left signals output by the sample-and-hold means are adjusted so that the noise components are substantially equal in level, and the right and left signals are supplied to the subtraction means. Accordingly, the noise components generated by sampling offset each other in the subtraction means, so that it is possible to remove the sampling noise of a wobble signal effectively, and to improve the performance of reproduction of ATIP information.

[0016]

[FORMS OF CARRYING OUT THE INVENTION]

FIG. 1 shows a block diagram of a first embodiment of the wobble signal detection circuit of the present invention. In FIG. 1, the same parts as those of FIG. 5 are referred to by the same numerals.

Here, the light beam spot 11 is emitted onto the pregroove 10 of a CD-R disk shown in FIG. 2, and its reflected beam is detected by the four divided detectors 12A, 12B, 12C, and 12D. The detection signals A, B, C, and D of these detectors 12A, 12B, 12C, and 12D, respectively, are supplied to the sample-and-hold circuit 14.

[0017]

The sample-and-hold circuit 14, which is supplied with a mode signal, is turned off in the first unrecorded disk reproduction mode and the third recorded disk

reproduction mode so as to let the supplied signals pass and to output them, and is turned on in the second reproduction-during-recording mode so as to output sampled and held signals. The signals A and B from the detectors 12A and 12B on the left side in the longitudinal direction of a track (that is, the pregroove 10), output by the sample-and-hold circuit 14, are added in the adder 16, and the signals C and D from the detectors 12C and 12D on the right side in the longitudinal direction of the track, output by the sample-and-hold circuit 14, are added in the adder 18.

[0018]

The output signals (A+B) and (C+D) of the adders 16 and 18, respectively, are supplied to lowpass filters (LPF) 40 and 42. Each of the LPFs 40 and 42, which is supplied with the mode signal, is turned off in the first unrecorded disk reproduction mode and the third recorded disk reproduction mode so as to let the supplied signal pass and to output it, and is turned on in the second reproduction-during-recording mode so as to cut off high-frequency components with, for example, a cutoff frequency of 24 kHz, exceeding a wobble signal of a frequency of 22.05±1 kHz. Sampling noise is a high-frequency component higher than or equal to a frequency of 200 kHz.

[0019]

In the first unrecorded disk reproduction mode and the third recorded disk reproduction mode, the output signals (A+B) and (C+D) of the adders 16 and 18, respectively, pass through the lowpass filters 40 and 42 to be supplied via the coupling capacitors C1 and C2 to the subtracter 20, where the output signal of the adder 18 is subtracted from the output signal (A+B) of the adder 16, so that a signal (A+B) - (C+D) is supplied to the terminal

a of the switch 22.

[0020]

In the first unrecorded disk reproduction mode, the terminal a of the switch 22 is selected. The output of the subtracter 20 is supplied to the bandpass filter (BPF) 24, where unnecessary frequency components are removed, and is further supplied via the coupling capacitor C3 to the highpass filter (HPF) 26, where unnecessary frequency components are removed. Thereafter, it is compared with the reference voltage Vref in the comparator 28, so that a binary wobble signal (A+B) - (C+D) is obtained and output from the terminal 32.

[0021]

On the other hand, in the third recorded disk reproduction mode, the lowpass filters 40 and 42 are turned off, and the terminal b of the switch 22 is selected. Here, the output signal of the adder 16 including an reproduced RF signal is supplied to the VCA (voltage-controlled amplifier) 34, while the output signal of the adder 18 including the reproduced RF signal is supplied to the VCA (voltage-controlled amplifier) 36. The AGC (automatic gain control circuit) 35 performs feedback control so that the amplitude of the output signal of the VCA 34 is at a predetermined level. Similarly, the AGC (automatic gain control circuit) 37 performs feedback control so that the amplitude of the output signal of the VCA 36 is at a predetermined level.

[0022]

The subtracter 38 subtracts the output signal (C+D+RF) of the VCA 36 from the output signal (A+B+RF) of the VCA 34. At this point, the reproduced RF signals equally included in the respective signals A, B, C, and D offset each other, and a signal (A+B) - (C+D) is supplied

to the terminal b of the switch 22.

In the third recorded disk reproduction mode, the terminal b of the switch 22 is selected, so that it is supplied to the bandpass filter 24, where unnecessary frequency components are removed, and is further supplied via the coupling capacitor C3 to the highpass filter 26, where unnecessary frequency components are removed. Thereafter, it is compared with the reference voltage Vref in the comparator 28, so that a binary wobble signal (A+B) - (C+D) is obtained and output from the terminal 32.

[0023]

Further, in the second reproduction-during-recording mode, the sample-and-hold circuit 14 and the lowpass filters 40 and 42 are turned on, and the terminal a of the switch 22 is selected. During recording, light beam power alternately repeats write power (a maximum value) and read power (a minimum value) as shown in FIG. 3(A), and the sample-and-hold circuit 14 samples and holds a signal of a reproduction level at the time of read power shown in FIG. 3(B) with an enlarged time axis at the rising of sampling pulses shown in FIG. 3(C).

[0024]

Here, the output signals of the sample-and-hold circuit 14 include sampling noise, so that the output signals of the adders 16 and 18 are as shown in FIGS. 3(D) and (E). However, after their respective sampling noises are removed by the lowpass filters 40 and 42, they are subjected to subtraction in the subtracter 20, so that a signal (A+B) - (C+D) including no sampling noise as shown in FIG. 3(F) is obtained.

[0025]

This signal is selected by the switch 22 so as to be supplied to the bandpass filter 24, where unnecessary

frequency components are removed. This signal is further supplied via the coupling capacitor C3 to the highpass filter 26, where unnecessary frequency components are removed. Thereafter, it is compared with the reference voltage Vref in the comparator 28, so that a binary wobble signal (A+B) - (C+D) is obtained and output from the terminal 32.

[0026]

Thus, it is possible to remove sampling noise included in a wobble signal effectively, and to improve the performance of reproduction of ATIP information at the time of recording, in particular, at the time of high-speed recording.

If the subtracter 20 were provided at a stage preceding a lowpass filter, the subtraction may cause the frequency of the sampling noise to shift to a lower frequency band, so that the sampling noise may not be removed with the lowpass filter. Accordingly, the lowpass filters 40 and 42 are provided at a stage preceding the subtracter 20. Further, a lowpass filter similar to the lowpass filters 40 and 42 may be provided at a stage preceding the adder for each signal.

[0027]

FIG. 4 shows a block diagram of a second embodiment of the wobble signal detection circuit according to the present invention. In FIG. 4, the same parts as those of FIG. 1 are referred to by the same numerals. In FIG. 4, the detection signals A, B, C, and D of the detectors 12A, 12B, 12C, and 12D are supplied to the sample-and-hold circuit 14.

The sample-and-hold circuit 14, which is supplied with a mode signal, is turned off in the first unrecorded disk reproduction mode and the third recorded disk

reproduction mode so as to let the supplied signals pass and to output them, and is turned on in the second reproduction-during-recording mode so as to output sampled and held signals. The signals A and B from the detectors 12A and 12B on the left side in the longitudinal direction of a track (that is, the pregroove 10), output by the sample-and-hold circuit 14, are added in the adder 16, and the signals C and D from the detectors 12C and 12D on the right side in the longitudinal direction of the track, output by the sample-and-hold circuit 14, are added in the adder 18.

[0028]

The output signals (A+B) and (C+D) of the adders 16 and 18, respectively, are supplied to gain adjustment circuits 50 and 52. Each of the gain adjustment circuits 50 and 52, which is supplied with the mode signal, is turned off in the first unrecorded disk reproduction mode and the third recorded disk reproduction mode so as to let the supplied signal pass and to output it, and is turned on in the second reproduction-during-recording mode.

[0029]

For instance, in a manufacturing process, the gain adjustment circuits 50 and 52 are subjected to gain adjustment, monitoring the output of the comparator 28 with a jittermeter, so that the jitter of the output of the comparator 28 is minimized. Therefore, the output levels of the gain adjustment circuits 50 and 52, including variations in the gains and offsets of the sample-and-hold circuit 14 and the adders 16 and 18, are set to be substantially the same.

[0030]

In the first unrecorded disk reproduction mode and the third recorded disk reproduction mode, the output

signals (A+B) and (C+D) of the adders 16 and 18, respectively, pass through the gain adjustment circuits 50 and 52 to be supplied via the coupling capacitors C1 and C2 to the subtracter 20, where the output signal of the adder 18 is subtracted from the output signal (A+B) of the adder 16, so that a signal (A+B) - (C+D) is supplied to the terminal a of the switch 22.

[0031]

In the first unrecorded disk reproduction mode, the terminal a of the switch 22 is selected. The output of the subtracter 20 is supplied to the bandpass filter 24, where unnecessary frequency components are removed, and is further supplied via the coupling capacitor C3 to the highpass filter 26, where unnecessary frequency components are removed. Thereafter, it is compared with the reference voltage Vref in the comparator 28, so that a binary wobble signal (A+B) - (C+D) is obtained and output from the terminal 32.

[0032]

On the other hand, in the third recorded disk reproduction mode, the gain adjustment circuits 50 and 52 are turned off, and the terminal b of the switch 22 is selected. Here, the output signal of the adder 16 including an reproduced RF signal is supplied to the VCA 34, while the output signal of the adder 18 including the reproduced RF signal is supplied to the VCA 36. The AGC 35 performs feedback control so that the amplitude of the output signal of the VCA 34 is at a predetermined level. Similarly, the AGC 37 performs feedback control so that the amplitude of the output signal of the VCA 36 is at a predetermined level.

[0033]

The subtracter 38 subtracts the output signal

(C+D+RF) of the VCA 36 from the output signal (A+B+RF) of the VCA 34. At this point, the reproduced RF signals equally included in the respective signals A, B, C, and D offset each other, and a signal (A+B) - (C+D) is supplied to the terminal b of the switch 22. In the third recorded disk reproduction mode, the terminal b of the switch 22 is selected, so that it is supplied to the bandpass filter 24, where unnecessary frequency components are removed, and is further supplied via the coupling capacitor C3 to the highpass filter 26, where unnecessary frequency components are removed. Thereafter, it is compared with the reference voltage Vref in the comparator 28, so that a binary wobble signal (A+B) - (C+D) is obtained and output from the terminal 32.

[0034]

Further, in the second reproduction-during-recording mode, the sample-and-hold circuit 14 and the gain adjustment circuits 50 and 52 are turned on, and the terminal a of the switch 22 is selected. During recording, light beam power alternately repeats write power (a maximum value) and read power (a minimum value) as shown in FIG. 3(A), and the sample-and-hold circuit 14 samples and holds a signal of a reproduction level at the time of read power shown in FIG. 3(B) with an enlarged time axis at the rising of sampling pulses shown in FIG. 3(C).

[0035]

Here, the output signals of the sample-and-hold circuit 14 include sampling noise, so that the output signals of the adders 16 and 18 are as shown in FIGS. 3(D) and (E). However, after the levels of their respective sampling noises are substantially equalized by the gain adjustment circuits 50 and 52, they are subjected to subtraction in the subtracter 20, so that a signal (A+B) -

(C+D) where the sampling noises offset each other as shown in FIG. 3(F) is obtained. This signal is selected by the switch 22 so as to be supplied to the bandpass filter 24, where unnecessary frequency components are removed. This signal is further supplied via the coupling capacitor C3 to the highpass filter 26, where unnecessary frequency components are removed. Thereafter, it is compared with the reference voltage Vref in the comparator 28, so that a binary wobble signal (A+B) - (C+D) is obtained and output from the terminal 32.

[0036]

Thus, it is possible to remove sampling noise included in a wobble signal effectively, and to improve the performance of reproduction of ATIP information at the time of recording, in particular, at the time of high-speed recording.

In the above-described embodiment, the gain adjustment circuits 50 and 52 are provided. Alternatively, only one of them may be provided, or a gain adjustment circuit may be provided for each of the four sample-and-hold outputs.

[0037]

In the above-described embodiments, a description is given, taking a CD-R disk, which is a write-once optical disk, as an example. However, it is also applicable to a rewritable optical disk as far as it is an optical disk on which an ATIP signal is recorded, and it is not limited to the above-described embodiments.

The detectors 12A, 12B, 12C, and 12D correspond to photodetection means recited in claims, the sample-and-hold circuit 14 corresponds to sample-and-hold means, the lowpass filters 40 and 42 correspond to lowpass filter means, the subtracter 20 corresponds to subtraction means,

and the gain adjustment circuits 50 and 52 correspond to gain adjustment means.

[0038]

[EFFECTS OF THE INVENTION]

As described above, the invention recited in claim 1 has, in a wobble signal detection circuit of an optical disk apparatus which detects a wobble signal by emitting a light beam spot onto a pregroove on an optical disk during recording and reproduction,

photodetection means for performing photodetection of each of right and left parts of the light beam spot divided in a longitudinal direction of a track, the light beam spot being emitted onto the optical disk;

sample-and-hold means for sampling and holding right and left detection signals detected by the photodetection means at a time of recording;

lowpass filter means for removing a noise component generated by the sampling from each of right and left signals output by the sample-and-hold means; and

subtraction means for obtaining the wobble signal by calculating a difference between right and left signals output by the lowpass filter means.

[0039]

Thus, at the time of recording, a sampling noise component is removed from each of right and left signals output by sample-and-hold means, and a wobble signal is calculated from the right and left signals. Accordingly, it is possible to remove the sampling noise of a wobble signal effectively, and to improve the performance of reproduction of ATIP information.

The invention recited in claim 2 has, in the wobble signal detection circuit of the optical disk apparatus as recited in claim 1,

gain adjustment means in place of said lowpass filter means, the gain adjustment means adjusting the noise components generated by sampling the right and left signals output by the sample-and-hold means so that the noise components are substantially equal in level, and supplying the right and left signals to the subtraction means.

[0040]

Thus, the noise components generated by sampling the right and left signals output by the sample-and-hold means are adjusted so that the noise components are substantially equal in level, and the right and left signals are supplied to the subtraction means. Accordingly, the noise components generated by sampling offset each other in the subtraction means, so that it is possible to remove the sampling noise of a wobble signal effectively, and to improve the performance of reproduction of ATIP information.

[BRIEF DESCRIPTION OF THE DRAWINGS]

[FIG. 1]

is a block diagram of a first embodiment of a wobble signal detection circuit of the present invention.

[FIG. 2]

shows a pregroove of a CD-R disk and four divided detectors.

[FIG. 3]

is a signal timing chart for explaining the present invention.

[FIG. 4]

is a block diagram of a second embodiment of the wobble signal detection circuit of the present invention.

[FIG. 5]

is a block diagram of a conventional wobble signal

detection circuit.

[FIG. 6]

is a signal timing chart for explaining a conventional example.

[DESCRIPTION OF THE REFERENCE NUMERALS]

10 pregroove

12A, 12B, 12C, 12D detectors

14 sample-and-hold circuit

16, 18 adders

20 subtracter

22 switch

24 bandpass filter (BPF)

26 highpass filter (HPF)

28 comparator

32 terminal

34, 36 VCAs (voltage-controlled amplifiers)

35, 37 AGCs (automatic gain control circuits)

38 subtracter

40, 42 lowpass filters

50, 52 gain adjustment circuits

[DOCUMENT NAME] ABSTRACT OF DISCLOSURE

[ABSTRACT]

[OBJECT] An object is to provide a wobble signal detection circuit of an optical disk unit which can effectively remove sampling noise from a wobble signal in the reproduction-during-recording mode and improve the performance of reproduction of ATIP information.

[MEANS OF SOLUTION] Sample-and-hold means 14 sampling and holding right and left detection signals detected in photodetection means at the time or recording; lowpass filter means 40 and 42 removing a noise component generated by sampling from each of right and left signals output by the sample-and-hold means; and subtraction means 20 obtaining a wobble signal by calculating the difference between right and left signals output by the lowpass filter means are included. Thus, a wobble signal is calculated by removing the sampling noise component of each of right and left signals at the time of recording. Accordingly, it is possible to remove the sampling noise of a wobble signal effectively, and to improve the performance of reproduction of ATIP information.

[SELECTED DRAWING]

FIG. 1

DOCKET NUMBER

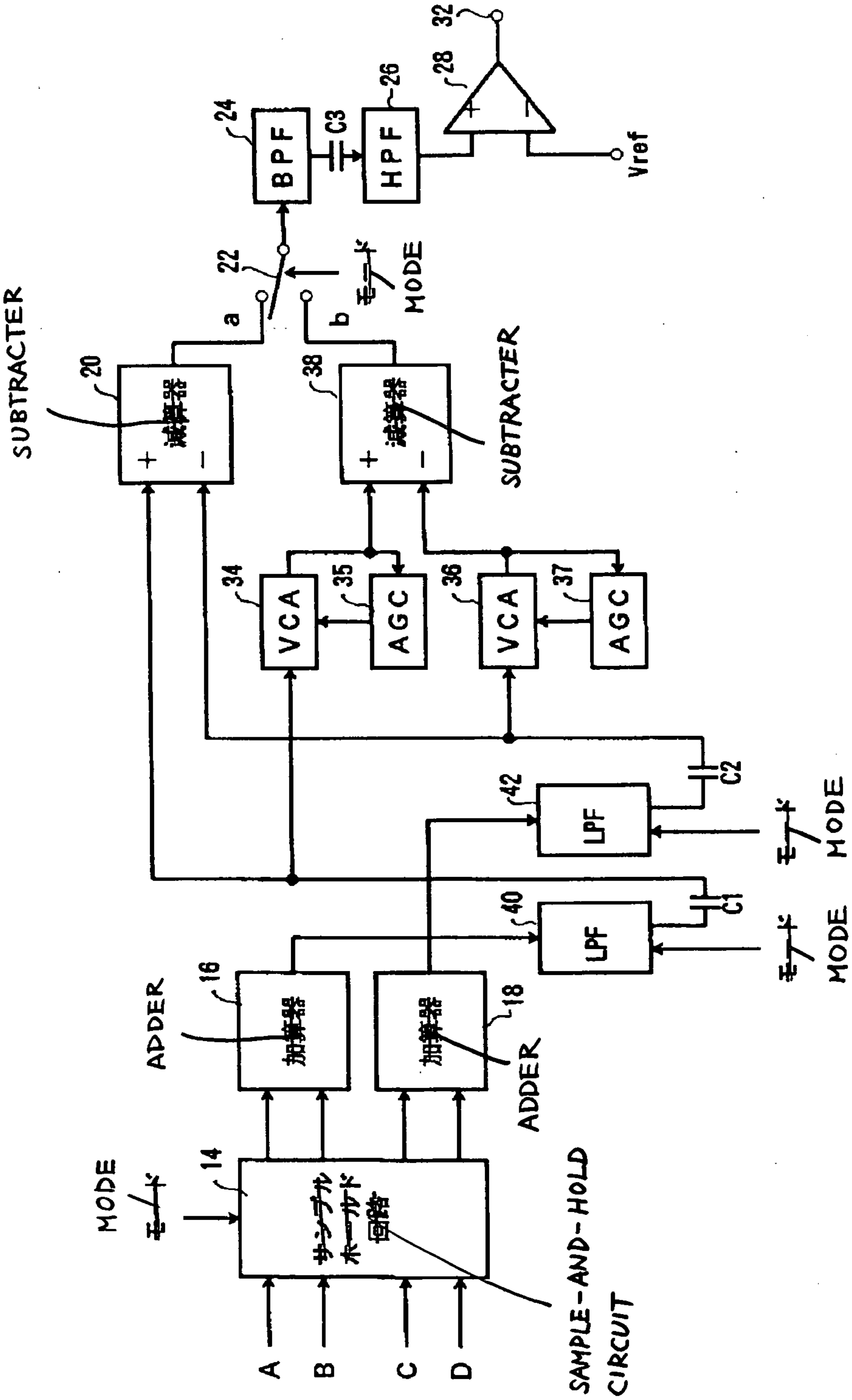
~~整理番号~~＝ＴＥＰ９９０５０５Ａ (1)

【~~書類名~~】 ~~図面~~ DRAWINGS

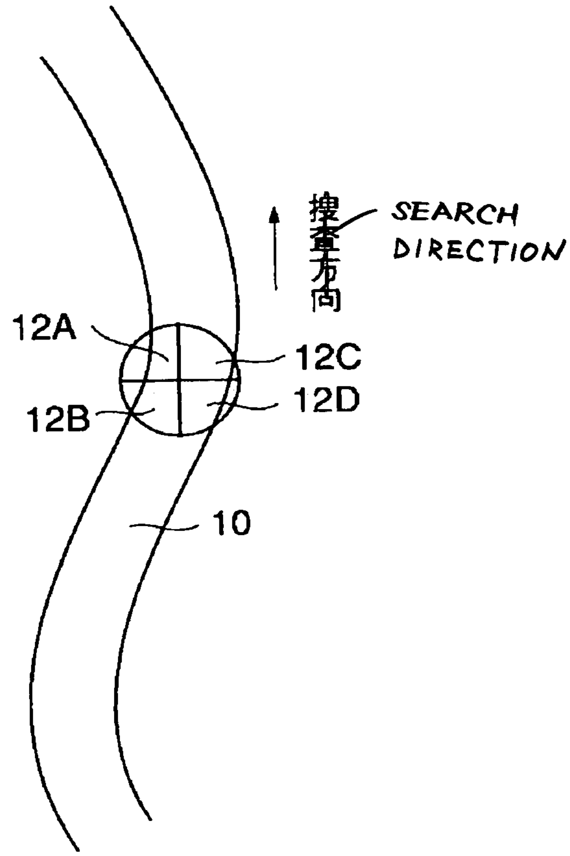
DOCUMENT NAME

【~~図1~~】

FIG. 1

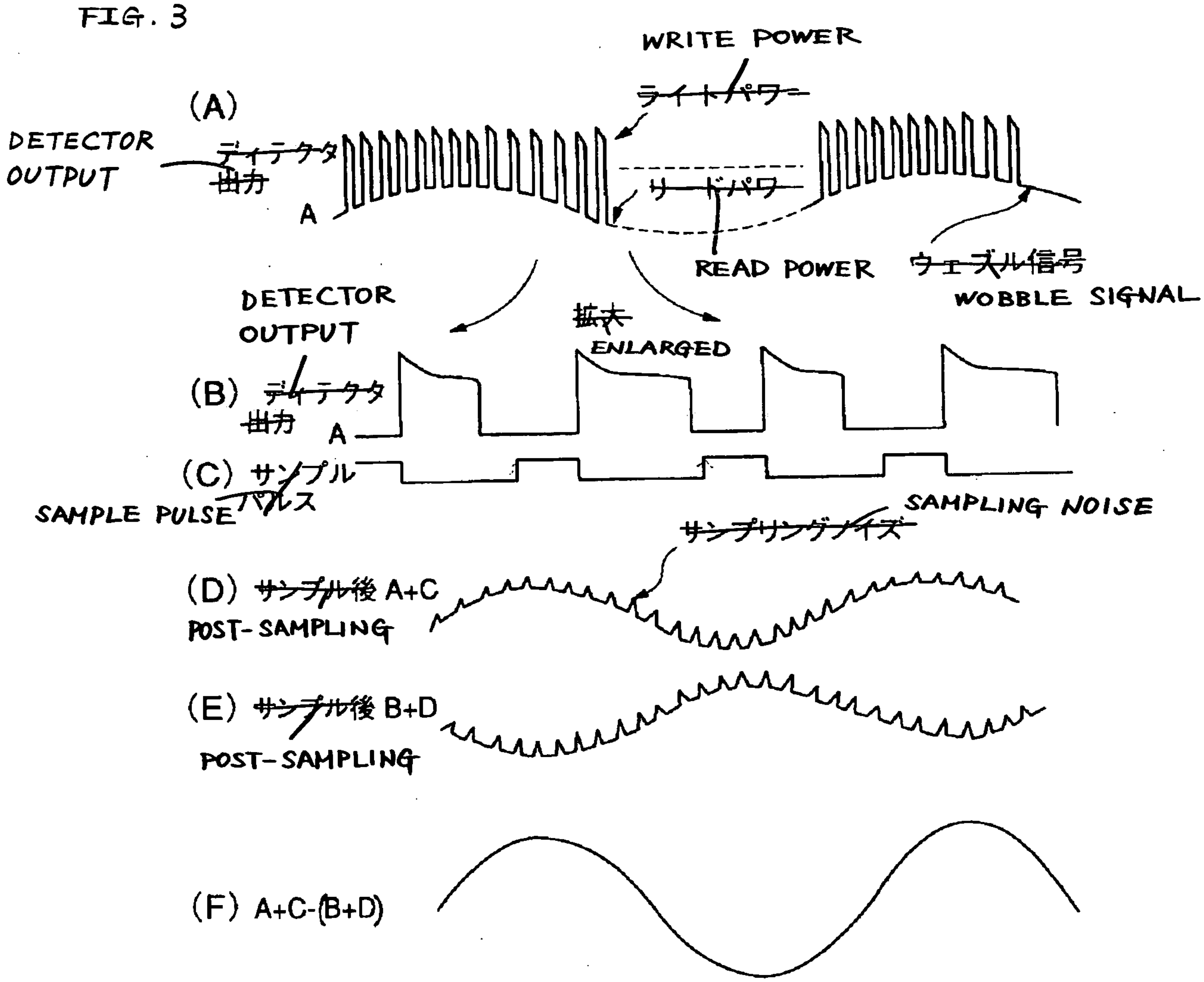


【~~図２~~】
FIG. 2

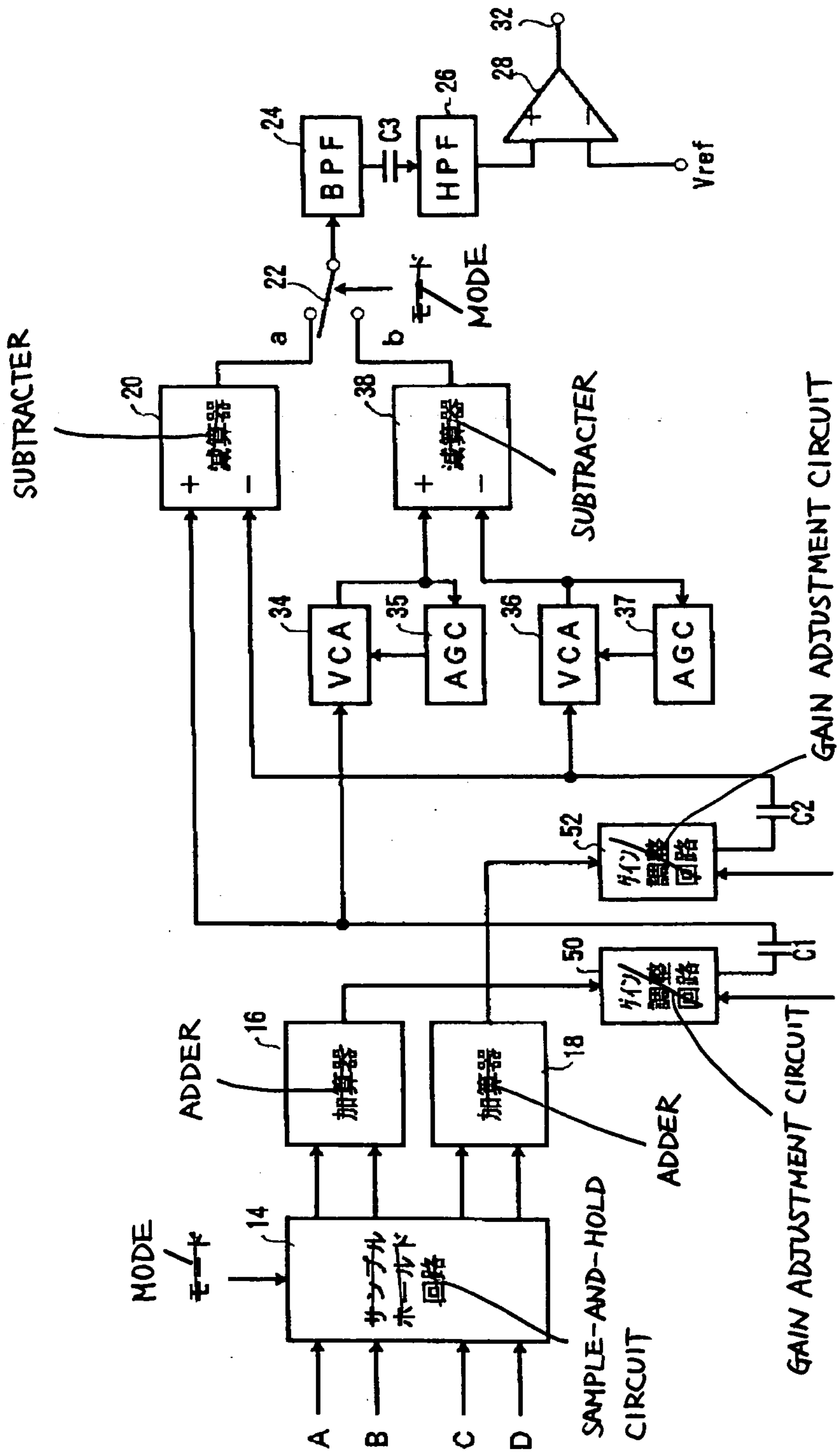


【~~図3~~】

FIG. 3

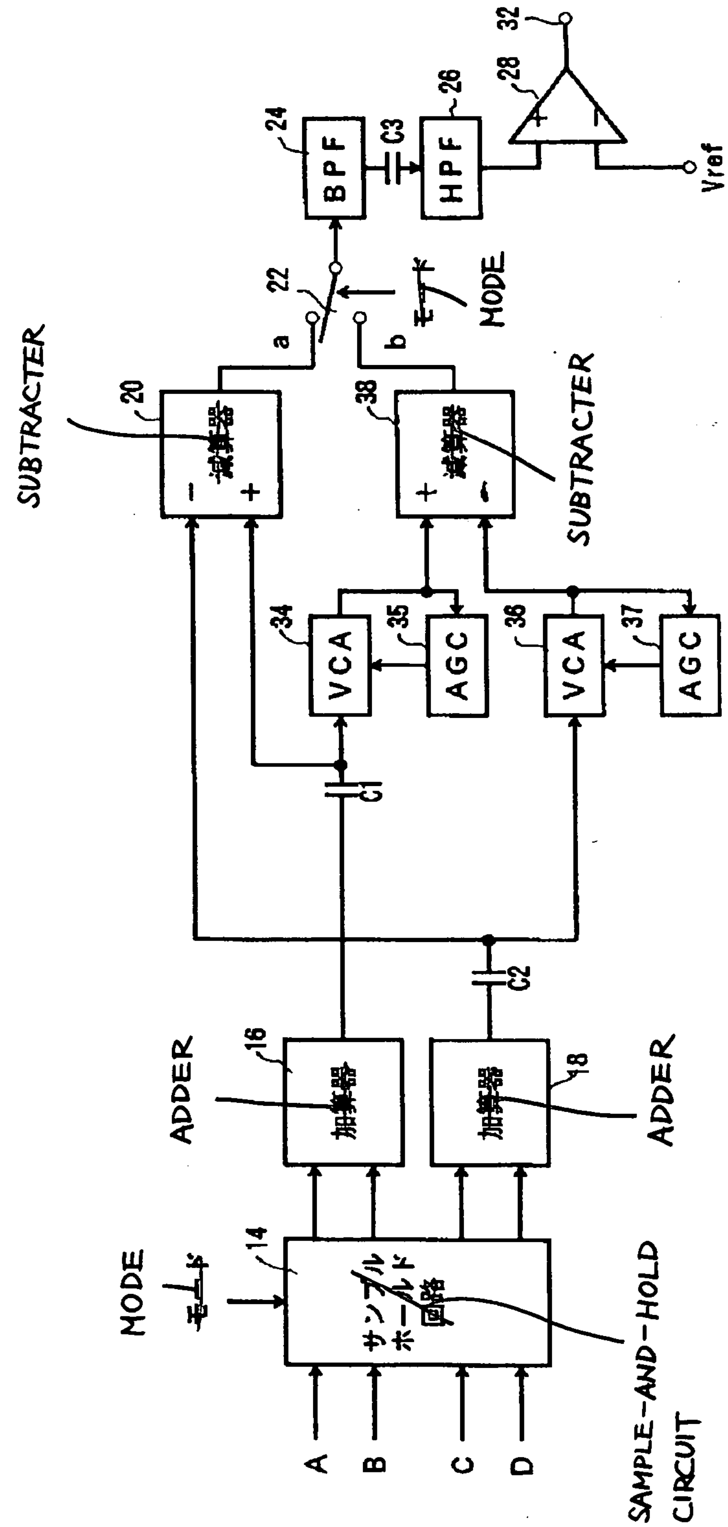

WRITE POWER
~~ライトパワー~~
(A)
DETECTOR OUTPUT
~~ディテクタ出力~~
A
~~リードパワー~~
READ POWER
~~ウォブル信号~~
WOBBLE SIGNAL
DETECTOR OUTPUT
~~拡大~~
ENLARGED
(B) ~~ディテクタ出力~~
A
(C) ~~サンプルパルス~~
SAMPLE PULSE
SAMPLING NOISE
~~サンプリングノイズ~~
(D) ~~サンプル後~~ A+C
POST-SAMPLING
(E) ~~サンプル後~~ B+D
POST-SAMPLING
(F) A+C-(B+D)

【~~図４~~】
FIG. 4


A
B
C
D
14
サンプル ホールド 回路
SAMPLE-AND-HOLD CIRCUIT
MODE
モード
16
加算器
ADDER
18
加算器
ADDER
50
ゲイン 調整 回路
GAIN ADJUSTMENT CIRCUIT
52
ゲイン 調整 回路
GAIN ADJUSTMENT CIRCUIT
C1
C2
34
VCA
35
AGC
36
VCA
37
AGC
20
減算器
SUBTRACTER
38
減算器
SUBTRACTER
a
b
22
24
BPF
C3
26
HPF
28
32
Vref

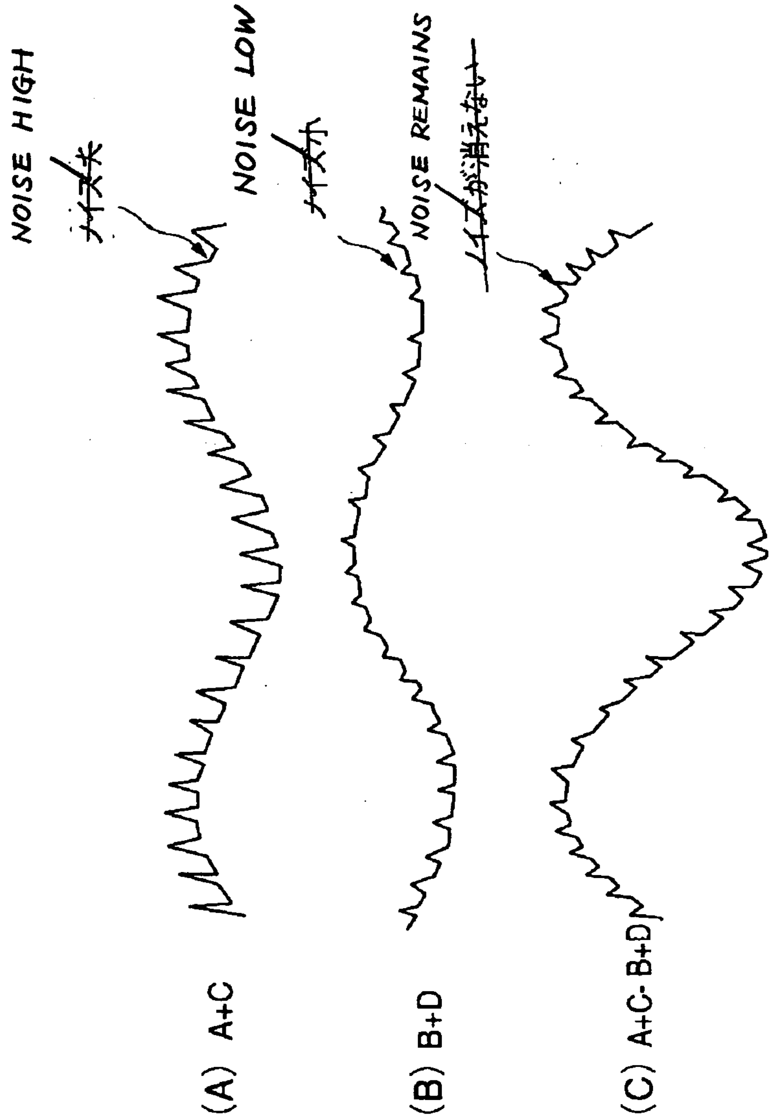
【~~図~~５】

FIG. 5


A
B
C
D
MODE
モード
14
サンプルホールド回路
SAMPLE-AND-HOLD CIRCUIT
16
加算器
ADDER
18
加算器
ADDER
C1
C2
34
VCA
35
AGC
36
VCA
37
AGC
20
減算器
SUBTRACTER
38
減算器
SUBTRACTER
a
b
22
モード
MODE
24
BPF
C3
26
HPF
28
32
Vref

【~~図6~~】

FIG. 6


NOISE HIGH
~~ノイズ大~~
NOISE LOW
~~ノイズ小~~
NOISE REMAINS
~~ノイズが消えない~~
(A) A+C
(B) B+D
(C) A+C- B+D